

Appl. No. 10/077,211  
Amtdt dated October 31, 2003

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application.

**Listing of Claims:**

Claim 1 (currently amended): Structure comprising:

a substrate formed of a heat deformable material;

at least one semiconductor die embedded in said substrate such that the top surface(s) of said at least one semiconductor die and the top surface of said substrate are in substantially the same plane;

a plurality of bonding pads formed on the top surface(s) of said at least one die; and

a plurality of conductive paths formed over the top surface(s) of said at least one die and the top surface of said substrate, each conductive path ending on the top surface of said substrate in a conductive land or pad and beginning in electrical contact with a corresponding bonding pad on said at least one die thereby to connect said corresponding bonding pad on the top surface(s) of said at least one die with a corresponding conductive land or pad on the top surface of said substrate;

wherein an opening in said substrate to hold said die is formed during embedding of said die in said substrate.

Claim 2 (original): Structure as in Claim 1 including a plurality of conductive balls, each ball being formed on a corresponding one of the conductive lands or pads on the top of said substrate, and conductive balls allowing said structure to be electrically connected to electrical contacts on an additional substrate.

SILICON VALLEY  
PATENT GROUP LLP  
3550 Mission College Blvd.  
Suite 200  
Santa Clara, CA 95051  
(408) 982-8210  
FAX: (408) 982-8210

Appl. No. 10/077,211  
Amtd dated October 31, 2003

Claim 3 (original): Structure as in Claim 2 wherein said additional substrate is a printed circuit board.

Claim 4 (original): Structure as in Claim 3 wherein said printed circuit board includes electrically conductive traces connected to said electrical contacts thereby to allow electrical signals to be sent from said at least one die to circuitry external to said at least one die and to also allow electrical signals to be sent from circuitry external to said at least one die to said at least one die.

Claim 5 (original): Structure as in Claim 1 wherein the top surface(s) of said at least one die is (are) protected by protective coating thereby to prevent contamination or moisture from reaching the top surface(s) of said at least one die and to act as a barrier between the semiconductor material and the conductive paths.

Claim 6 (currently amended): Structure as in Claim 5 wherein said protective coating is selected from the group of materials consisting of plastic, polyimide and other photosensitive polymers.

Claim 7 (original): Structure as in Claim 5 wherein said protective coating covers the top surface(s) not only of said at least one die but also of said substrate.

Claim 8 (original): Structure as in Claim 1 including  
a second set of bonding pads on a bottom surface of said substrates opposite to the top surface of said substrate; and

SILICON VALLEY  
PATENT GROUP LLC  
1350 Mission College Road  
Suite 300  
Santa Clara, CA 95054  
(408) 982-8200  
FAX: (408) 982-8210

Appl. No. 10/077,211  
Amtd: dated October 31, 2003

a set of conductive vias in said substrate, each conductive via connecting one of the bonding pads on the bottom surface of said substrate to a corresponding bonding pad on the top surface of said substrate.

Claim 18 (original): Structure as in Claim 1, including:

at least one conductive plane formed over at least a portion of at least one top surface of said at least one die, said conductive plane being electrically insulated from selected ones of said plurality of bonding pads formed on the top surface of said at least one die.

Claim 19 (original): Structure as in Claim 18 wherein said conductive plane is formed in a region interior to said plurality of bonding pads on at least one top surface of said at least one die.

Claim 20 (original): Structure as in Claim 19 wherein said conductive plane is connected to one or more selected electrical contacts so as to be capable of providing a voltage from the group of voltages consisting of ground and  $V_{cc}$ .

Claim 21 (original): Structure as in Claim 19 wherein said conductive plane has at least one connection to at least one of the bonding pads formed on the at least one top surface of said at least one die thereby to allow a selected potential to be applied to said conductive plane.

Claim 22 (original): Structure as in Claim 18 wherein:

SILICON VALLEY  
PATENT GROUP LLP  
3330 Mission College Blvd.  
Suite 300  
Santa Clara, CA 95051  
(408) 982-8210  
FAX (408) 982-8210

Appl. No. 10/077,211  
Amdt dated October 31, 2003

said at least one conductive plane has formed over the top surface thereof a protective coating of an insulating material;

at least one opening is formed through said protective coating of insulating material to expose a portion of the top surface of said conductive plane; and

a conductive material is placed in said opening to allow both electrical connection to be made to said conductive plane and to allow heat to be transferred from said conductive plane.

Claim 23 (original): Structure as in Claim 22 wherein:

said protective coating has a plurality of openings formed in the top surface thereof and a plurality of conductive materials formed in said corresponding plurality of openings, each conductive material in a selected opening being capable of providing electrical connection to said conductive plane and allowing heat to be transferred from said conductive plane to an external sink or substrate.

Claim 24 (original): Structure as in Claim 23 wherein:

said conductive material comprises lead balls formed in each of said openings in said protective coating, said lead balls being capable of being connected to a printed circuit board, thereby to allow electrical potential to be applied to said conductive plane and heat to be transferred from said conductive plane.

Claim 25 (original): Structure as in Claim 18, including:

a bottom electrically conductive plane formed on the surface of said substrate opposite said top surface.

SILICON VALLEY  
PATENT GROUP LLP  
1330 Mission College Blvd  
Suite 200  
San Jose, CA 95054  
(408) 982-8200  
FAX (408) 982-8210

Appl. No. 10/077,211  
Amdt dated October 31, 2003

Claim 26 (original): Structure as in Claim 25, including:

at least one electrically conductive connection formed to connect said bottom electrically conductive plane to a source of electrical potential.

Claim 27 (original): Structure as in Claim 26 wherein said source of electrical potential is selected from a group of voltage sources capable of providing ground and Vcc.

Claim 28 (currently amended) Structure comprising:

a substrate formed of a heat deformable materials material;

a semiconductor die embedded in said substrate such that the top surface of said semiconductor die and the top surface of said substrate are both exposed;

a plurality of bonding pads formed on the top surface of said semiconductor die; and

a plurality of conductive paths formed over the top surface of said substrate, each conductive path ending on said top surface of said substrate as a conductive land, and beginning on said semiconductor die in electrical contact with one of said plurality of bonding pads;

wherein an opening in said substrate to hold said die is formed during embedding of said die in said substrate.

Claim 29 (original): Structure as in claim 20 wherein:

the top surface of said semiconductor die and the top surface of said substrate are substantially coplanar.

Claim 30 (new): Structure comprising:

a substrate formed of a heat deformable material;

SILICON VALLEY  
PATENT GROUP LLP  
1300 International College Village  
Suite 500  
Annex, Orange, CA 92664  
(415) 961-5111  
Fax: (415) 961-5112

Appl. No. 10/077,211  
Amtd dated October 31, 2003

at least one semiconductor die embedded in said substrate such that the top surface(s) of said at least one semiconductor die and the top surface of said substrate are in substantially the same plane;

a plurality of bonding pads formed on the top surface(s) of said at least one die; and  
a plurality of traces of conductive material formed over the top surface(s) of said at least one die and the top surface of said substrate, each trace beginning in electrical contact with a corresponding bonding pad on said at least one die, and each trace ending on the top surface of said substrate in a conductive land or pad and being integrally formed on said substrate, each trace electrically connecting said corresponding bonding pad on the top surface(s) of said at least one die with said corresponding conductive land or pad on the top surface of said substrate.

Claim 31 (new): Structure as in Claim 30 including a plurality of conductive balls, each ball being formed on a corresponding one of the conductive lands or pads on the top of said substrate, and conductive balls allowing said structure to be electrically connected to electrical contacts on an additional substrate.

Claim 32 (new): Structure as in Claim 31 wherein said additional substrate is a printed circuit board.

Claim 33 (new): Structure as in Claim 32 wherein said printed circuit board includes electrically conductive traces connected to said electrical contacts thereby to allow electrical signals to be sent from said at least one die to circuitry external to said at least one die and to also allow electrical signals to be sent from circuitry external to said at least one die to said at least one die.

Claim 34 (new): Structure as in Claim 30 wherein the top surface(s) of said at least one die is (are) protected by protective coating thereby to prevent contamination or

SILICON VALLEY  
PATENT GROUP LLP  
1750 Inland College Way  
Suite 300  
Sunnyvale, CA 95054  
(408) 982-8210  
FAX (408) 982-8210

Appl. No. 10/077,211  
Amdt dated October 31, 2003

moisture from reaching the top surface(s) of said at least one die and to act as a barrier between the semiconductor material and the conductive paths.

Claim 35 (new): Structure as in Claim 34 wherein said protective coating is selected from the group of materials consisting of plastic, polyimide and photosensitive polymers.

Claim 36 (new): Structure as in Claim 34 wherein said protective coating covers the top surface(s) not only of said at least one die but also of said substrate.

Claim 37 (new): Structure as in Claim 30 including

a second set of bonding pads on a bottom surface of said substrates opposite to the top surface of said substrate; and

a set of conductive vias in said substrate, each conductive via connecting one of the bonding pads on the bottom surface of said substrate to a corresponding bonding pad on the top surface of said substrate.

Claim 38 (new): Structure as in Claim 30, including:

at least one conductive plane formed over at least a portion of at least one top surface of said at least one die, said conductive plane being electrically insulated from selected ones of said plurality of bonding pads formed on the top surface of said at least one die.

Claim 39 (new): Structure as in Claim 38 wherein said conductive plane is formed in a region interior to said plurality of bonding pads on at least one top surface of said at least one die.

Appl. No. 10/077,211  
Amdt dated October 31, 2003

Claim 40 (new): Structure as in Claim 39 wherein said conductive plane is connected to one or more selected electrical contacts so as to be capable of providing a voltage from the group of voltages consisting of ground and Vcc.

Claim 41 (new): Structure as in Claim 39 wherein said conductive plane has at least one connection to at least one of the bonding pads formed on the at least one top surface of said at least one die thereby to allow a selected potential to be applied to said conductive plane.

Claim 42 (new): Structure as in Claim 38 wherein:

said at least one conductive plane has formed over the top surface thereof a protective coating of an insulating material;

at least one opening is formed through said protective coating of insulating material to expose a portion of the top surface of said conductive plane; and

a conductive material is placed in said opening to allow both electrical connection to be made to said conductive plane and to allow heat to be transferred from said conductive plane.

Claim 43 (new): Structure as in Claim 42 wherein:

said protective coating has a plurality of openings formed in the top surface thereof and a plurality of conductive materials formed in said corresponding plurality of openings, each conductive material in a selected opening being capable of providing electrical connection to said conductive plane and allowing heat to be transferred from said conductive plane to an external sink or substrate.

SILICON VALLEY  
PATENT GROUP LLP  
3500 Ardenway College Blvd.  
Suite 500  
San Jose, CA 95128  
(408) 982-8210  
FAX (408) 982-8222



Appl. No. 10/077,211  
Amdt dated October 31, 2003

Claim 44 (new): Structure as in Claim 43 wherein:

said conductive material comprises lead balls formed in each of said openings in said protective coating, said lead balls being capable of being connected to a printed circuit board, thereby to allow electrical potential to be applied to said conductive plane and heat to be transferred from said conductive plane.

Claim 45 (new): Structure as in Claim 38, including:

a bottom electrically conductive plane formed on the surface of said substrate opposite said top surface.

Claim 46 (new): Structure as in Claim 45, including:

at least one electrically conductive connection formed to connect said bottom electrically conductive plane to a source of electrical potential.

Claim 47 (new): Structure as in Claim 46 wherein said source of electrical potential is selected from a group of voltage sources capable of providing ground and  $V_{cc}$ .

Claim 48 (new): Structure comprising:

a substrate formed of a heat deformable material;

a semiconductor die embedded in said substrate such that the top surface of said semiconductor die and the top surface of said substrate are both exposed;

a plurality of bonding pads formed on the top surface of said semiconductor die; and

a plurality of traces of conductive material formed over the top surface of said substrate, each trace ending on said top surface of said semiconductor die at one of said

SILICON VALLEY  
PATENT GROUP LLP

2180 Mission College Blvd.  
Suite 301  
Santa Clara, CA 95050  
(408) 982-8210  
FAX (408) 982-8219

Appl. No. 10/077,211  
Amtd dated October 31, 2003

a plurality of bonding pads formed on the top surface of said semiconductor die; and  
a plurality of traces of conductive material formed over the top surface of said substrate, each trace ending on said top surface of said semiconductor die at one of said plurality of bonding pads and each trace starting on said top surface of said substrate as a conductive land and integrally formed thereon.

Claim 49 (new): Structure as in claim 48 wherein:  
the top surface of said semiconductor die and the top surface of said substrate are substantially coplanar.

SILICON VALLEY  
PATENT GROUP LLP  
36 Mountain College Road  
Suite 200  
Sunnyvale, CA 94086  
COURT FILED  
FAX (408) 982-8210